CLAIMS

The invention claimed is:

1. A semiconductor package, comprising:

a interposer construction containing only a single dielectric support member and comprising one or more conductive circuit traces contacting the single dielectric support member;

a semiconductor die electrically connected with at least one of the traces; and

the circuit traces being between the semiconductor die and the dielectric support member.

2. The semiconductor package of claim 1 wherein the dielectric support member is a photomask material.

3. The semiconductor package of claim 1 wherein the dielectric support member is not a photomask material.

4. The semiconductor package of claim 1 wherein the one or more circuit traces comprise copper.

5. The semiconductor package of claim 1 wherein the dielectric support member is patterned to have openings extending therein, the package further comprising one or more electrically-conductive connectors within one or more of the openings and in electrical connection with the one or more circuit traces.

6. The semiconductor package of claim 5 wherein the electrically-conductive connectors are solder balls.

7. The semiconductor package of claim 1 wherein the dielectric support member is patterned to have openings extending therein, the package further comprising:

contact pads within one or more of the openings and in electrical connection with the one or more circuit traces; and

solder balls in electrical connection with the contact pads.

8. The semiconductor package of claim 1 wherein:

the dielectric support member has a slit extending therethrough;

the dielectric support member has one or more openings extending therethrough for electrical connection to the one or more circuit traces; and

the electrical connection of the semiconductor die to said at least one of the circuit traces includes one or more wire bonds extending from the die, through the slit, and into at least one of the openings.

9. A semiconductor package, comprising:

a patterned substrate having openings extending therethrough;

conductive circuit traces over the substrate and having portions extending over the openings;

a semiconductor die over the circuit traces; and

a homogenous matrix contacting the circuit traces and also contacting the die.

10. The semiconductor package of claim 9 wherein the patterned substrate comprises polyimide.

11. The semiconductor package of claim 9 wherein the patterned substrate comprises a photomask.

12. The semiconductor package of claim 9 wherein the patterned substrate consists of a photomask.

13. The semiconductor package of claim 9 wherein the patterned substrate consists of a dry film photomask.

14. The semiconductor package of claim 9 wherein the matrix is a cured paste.

15. The semiconductor package of claim 9 wherein the matrix is a polymeric matrix.

16. The semiconductor package of claim 9 wherein the circuit traces comprise patterned copper-containing material.

17. The semiconductor package of claim 9 further comprising solder balls extending within the openings and in electrical contact with the circuit traces.

18. A semiconductor package, comprising:

a patterned substrate having openings extending therethrough;

conductive circuit traces over the substrate and having portions extending over the openings;

a semiconductor die over the circuit traces; and

an adhesive structure touching the circuit traces and also touching the die.

19. The semiconductor package of claim 18 wherein the patterned substrate comprises polyimide.

20. The semiconductor package of claim 18 wherein the patterned substrate comprises a photomask.

21. The semiconductor package of claim 18 wherein the patterned substrate consists of a photomask.

22. The semiconductor package of claim 18 wherein the patterned substrate consists of a dry film photomask.

23. The semiconductor package of claim 18 wherein the adhesive structure comprises a polymeric matrix which touches both the circuit traces and the die.

24. The semiconductor package of claim 18 wherein the adhesive structure comprises a tape having opposing sides and adhesive provided on the opposing sides.

25. The semiconductor package of claim 18 wherein the circuit traces comprise patterned copper-containing material.

26. The semiconductor package of claim 18 further comprising solder balls extending within the openings and in electrical contact with the circuit traces.

27. The semiconductor package of claim 26 further comprising electrically conductive contact pads between the solder balls and the circuit traces, the electrically conductive contact pads including a nickel-containing layer proximate the circuit traces and a gold-containing layer proximate the solder balls.

28. The semiconductor package of claim 18 further comprising a slit extending through the substrate and one or more wire bonds extending from the die, through the slit, and into one or more of the openings through the substrate to electrically connect with one or more of the circuit traces.

29. A method of forming a semiconductor package, comprising:

laminating an electrically-conductive layer to a masking material, the electrically-conductive layer having a first surface facing the masking material and a second surface in opposing relation to the first surface;

patterning the masking material to form openings extending to the first surface of the electrically-conductive layer;

patterning the electrically-conductive layer into one or more circuit traces; and

while the patterned electrically-conductive layer remains laminated only to the masking material, providing an integrated circuit die over the second surface of the patterned electrically-conductive layer.

30. The method of claim 29 wherein the patterning the masking material occurs before the patterning the electrically-conductive layer.

31. The method of claim 29 wherein the masking material is a photomask film and the patterning of the masking material comprises photolithographic processing of the photomask film.

32. The method of claim 29 wherein the masking material is a dielectric material, and wherein the patterning of the masking material comprises formation of a patterned photomask over the dielectric material and transferring of a pattern from the patterned photomask to the dielectric material.

33. The method of claim 29 wherein the electrically-conductive layer comprises copper.

34. The method of claim 29 wherein the electrically-conductive layer consists essentially of copper.

35. The method of claim 29 wherein the electrically-conductive layer consists of copper.

36. The method of claim 29 further comprising forming electrically-conductive contact pads on the first surface of the electrically-conductive layer within the openings in the patterned masking material, and forming electrically-conductive connectors in electrical connection with the electrically-conductive contact pads.

37. A method of forming a semiconductor package, comprising:

providing a construction having an electrically-conductive expanse over an insulative-material substrate, the electrically-conductive expanse having a first surface facing the substrate and a second surface in opposing relation to the first surface;

forming a pattern of openings which extend through the substrate to expose regions of the first surface of the electrically-conductive expanse;

plating contact pad material onto the exposed regions of the first surface of the electrically-conductive expanse;

patterning the electrically-conductive expanse into one or more circuit traces, the circuit traces comprising said second surface;

providing a dielectric material in direct contact with the second surface of one or more of the circuit traces; and

providing an integrated circuit die over the dielectric material.

38. The method of claim 37 wherein the providing the dielectric material comprises providing a tape having adhesive on opposing sides, one of said opposing sides being provided in the direct contact with said second surface of the one or more circuit traces and another of the opposing sides being provided in direct contact with the integrated circuit die.

39. The method of claim 37 wherein the providing the dielectric material comprises providing a liquid between the integrated circuit die and the one or more circuit traces, and curing the liquid to form a dielectric matrix.

40. The method of claim 37 wherein the dielectric material is a glue.

41. The method of claim 37 wherein the insulative-material substrate comprises polyimide.

42. The method of claim 37 wherein the insulative-material substrate comprises a photomask.

43. The method of claim 37 wherein the insulative-material substrate consists of a photomask.

44. The method of claim 37 wherein the insulative-material substrate consists of a dry film photomask.

45. The method of claim 44 wherein the forming the pattern of openings comprises exposing the substrate to patterned radiation and subsequently exposing the substrate to a developer.

46. The method of claim 37 wherein the electrically-conductive expanse comprises copper.

47. The method of claim 37 wherein the electrically-conductive expanse consists essentially of copper.

48. The method of claim 37 wherein the electrically-conductive expanse consists of copper.

49. The method of claim 37 wherein the electrically-conductive expanse is homogeneous.

50. The method of claim 37 wherein the patterning the electrically-conductive expanse into one or more circuit traces comprises:

formation of a patterned mask over the electrically-conductive expanse, the patterned mask covering a first portion of the electrically-conductive expanse while leaving a second portion exposed; and

subjecting said exposed second portion to etching conditions which remove said second portion while leaving the first portion of the expanse remaining over the substrate; the remaining first portion including the one or more circuit traces.

51. The method of claim 50 wherein the patterned mask remains over said one or more circuit traces as part of the dielectric material provided in direct contact with the second surface of said one or more circuit traces.

52. The method of claim 50 wherein the patterned mask is removed from over said one or more circuit traces prior to forming the dielectric material in direct contact with said one or more circuit traces.

53. The method of claim 37 wherein the plating the contact pad material comprises plating a nickel-containing material onto said exposed regions of the first surface of the electrically-conductive expanse and plating a gold-containing material onto the nickel-containing material.

54. The method of claim 37 wherein the contact pad material forms a plurality of contact pads, and further comprising:

after the plating of the contact pad material and the patterning of the electrically-conductive expanse into the one or more circuit traces, forming a slit extending through the insulative-material substrate; and

forming one or more wire bonds extending from the semiconductor die, through the slit and into electrical contact with the one or more of the contact pads.

55. The method of claim 37 wherein:

the electrically-conductive expanse comprises copper,

the insulative-material substrate comprises a dry film photomask, and

the providing the construction having the electrically-conductive expanse over the insulative-material substrate comprises laminating the dry film photomask and electrically-conductive expanse to one another.

56. The method of claim 37 wherein the electrically-conductive expanse comprises copper, the insulative-material substrate comprises a polyimide or glass weave core, and the providing the construction having the electrically-conductive expanse over the insulative-material substrate comprises:

providing a structure having the polyamide or glass weave core sandwiched between a pair of copper-containing layers; and

removing one of the copper-containing layers to form the construction.